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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,773	09/26/2003	Bunsho Kuramori	030712-13	4336

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
12/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,773	KURAMORI ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-10* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/RCE

The RCE and amendment submitted on Nov 3, 2008 were reviewed and considered with the following results:

The RCE was approved and entered.

Due to the decision by the Board of Appeals mailed on Sep 3, 2008, the rejections of claims 1-6 under 35 U.S.C. 112, first paragraph, as described on pages 4-5 of the previous Office Action (mailed prior to the Appeal Brief and Examiner's Answer), have been withdrawn. Also related to the board's decision, the objections to the title, abstract, and disclosure described on pages 3-4 of the previous Office Action have been withdrawn.

Amended claims 1-3, 7, and 9, and some comments within the board's decision, overcame the rejections of claims 1-10 under 35 U.S.C. 112, second paragraph as described on pages 5-6 of the previous Office Action. Therefore, those claim rejections have also been withdrawn.

Although page 7 of the previous Office Action had indicated claim 7-10 would be allowable if their rejections under 35 U.S.C. 112, second paragraph were overcome, this indication has now been withdrawn. After reconsidering the claimed limitations, and searching/ considering various prior art references, it is now believed the use of a six transistor level shift circuit, having two transistors with a gate oxide thickness thicker (or thinner) than two other associated transistors, appears to be an obvious type modification of known six transistor level shift circuits. Therefore, claims 7-10 are now rejected under prior art, as well as claims 1-3 and 5-6. These rejections are described later under their appropriate section.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Brox et al. (Brox). Fig. 2 shows a substrate voltage generating circuit comprising a first power supply node (e.g. see the sources of P1 and P2) supplied with first potential level VDD; a second power supply node (see the source of transistor 2) supplied with a second potential level (i.e. the unlabeled ground); output node OUT (i.e. the output of block 1) having third potential level VNEG lower than the second potential level; level shift circuit P1-P2,N1-N2 coupled between the first power supply node and the output node, and receiving a first input signal (i.e. the unlabeled output of logic gate 4) and a second input signal (i.e. the unlabeled output of inverter 9) complementary to the first input signal, wherein the level shift circuit outputs output signal "and connect" (i.e. supplied to the gate of 2) having the first and third potential levels; and switch circuit 2 which connects the second power supply node to the output node in response to the output signal from the level shift circuit. This anticipates claim 1. Since the second potential is ground, it is 0 volts. and claim 5 is anticipated. Third potential level VNEG is a negative voltage level, anticipating claim 6.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (Tanaka). Fig. 5a of Tanaka shows a voltage level shifting circuit comprising first-sixth transistors (i.e. 400-405 respectively); first/second potential levels VDD/VSSQ; input signal "ino"; and a complement "inob" of the input signal, wherein these transistors, levels, and signals directly correspond to the applicants' own Fig. 2's structure that comprises first-sixth transistors (i.e. P1,P2,N1-N4 respectively); first/second potential levels VDD/VBB; input signal IN; and a complement /IN of the input signal.. Therefore, it is not necessary to described all of the detailed connections here. However, the reference does not show/disclose the fifth/sixth transistors (i.e. 404/405) having a thickness of their gate oxide film at a second thickness thinner than a first thickness of the gate oxide film of the third/fourth transistors. It would have been obvious to one of ordinary skill in the art to have the fifth/sixth transistors 404/405 to each have a gate oxide film at a second thickness thinner than a first thickness of the gate oxide films of the third/fourth transistors 402/403, rendering claim 7 obvious. The third/fourth transistors receive their

corresponding input signal (i.e. "ino" or "inob") directly, wherein the fifth/sixth transistors do not receive either of these alternating input signals. Therefore, it is not necessary for the fifth/sixth transistors to have a thick second thickness that would help ensure the fifth/sixth transistors can withstand the alternating levels of the input signal(s). Since first potential level VDD is positive, and second potential level VSSQ is negative (e.g. see column 6, lines 8-12), claim 8 is also rendered obvious.

Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokai. Fig. 26 of Tokai shows a voltage level shifting circuit comprising first-sixth transistors (i.e. f1,f3,f2, f4,f13,f14 respectively); first/second potential levels Vdd/Vbb; input signal D; and complement ND of the input signal, wherein these transistors, levels, and signals directly correspond to the applicants' own Fig. 3's structure that comprises first-sixth transistors (i.e. P31,P32,N31-N34 respectively); first/second potential levels VDD/VBB; input signal IN; and complement /IN of the input signal. Therefore, it is not necessary to described all of the detailed connections here. However, the reference does not show/disclose the fifth/sixth transistors (i.e. f13/f14) having a second thickness of their gate oxide film thicker than a first thickness of the gate oxide film of the third/fourth transistors. It would have been obvious to one of ordinary skill in the art to have the fifth/sixth transistors f13/f14 have a thickness of their gate oxide file at a second thickness thicker than a first thickness of the gate oxide films of the third/fourth transistors f2/f4, rendering claim 9 obvious. The fifth/sixth transistors receive their corresponding input signal (i.e. D or ND) directly, wherein the third/fourth transistors do not receive either of these alternating input signals. Therefore, it is not necessary for the third/fourth transistors to have a thick first thickness that would help ensure the third/fourth transistors can withstand the alternating levels

of the input signal(s). . Since first potential level VDD is positive, and second potential level Vbb is negative, claim 10 is also rendered obvious.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brox et al. (Brox) as applied to claim 1 above, and further in view of Tanaka et al. (Tanaka). As previously described above, Brox shows/discloses a substrate voltage generating circuit comprising the first-third potential levels, level shift circuit, and switch circuit as cited within claim 1. However, the level shift circuit of Brox is shown as a four transistor circuit, instead of a six transistor level shift circuit. Tanaka shows a six transistor level shift circuit 400-405 in Fig. 5a that is coupled between positive first potential level VDD and negative third potential level VSSQ. Therefore, it would have been obvious to one of ordinary skill in the art to replace Brox's four transistor level shift circuit P1-P2,N1-N2 with Tanaka's six transistor level shift circuit. With the fifth/sixth transistors of Tanaka's level shift circuit having a second thickness thinner than a first thickness of the third/fourth transistors (for the same reasoning as previously described above with respect to the rejections of claims 7-8), claim 2 is rendered obvious. Replacing one type of level shift circuit (e.g. one having four transistors) with another functionally equivalent type of level shift circuit (e.g. one having six transistors) is well known to those of ordinary skill in the art.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brox et al. (Brox) as applied to claim 1 above, and further in view of Tokai. As previously described above, Brox shows/discloses a substrate voltage generating circuit comprising the first-third potential levels, level shift circuit, and switch circuit as cited within claim 1. However, the level shift circuit of Brox is shown as a four transistor circuit, instead of a six transistor level shift circuit. Tokai shows a four transistor level shift circuit f1,f3,f2,f14 in Fig. 26, and a functionally equivalent six

transistor level shift circuit f1,f3,f2,f4,f13,f14 in Fig. 27, wherein both of these level shift circuits are coupled between positive first potential level Vdd and negative third potential level Vbb. Therefore, it would have been obvious to one of ordinary skill in the art to replace Brox's four transistor level shift circuit P1-P2,N1-N2 with Tanaka's six transistor level shift circuit. With the fifth/sixth transistors of Tokai's level shift circuit having a second thickness thicker than a first thickness of the third/fourth transistors (for the same reasoning as previously described above with respect to the rejections of claims 9-10), claim 3 is rendered obvious. Replacing one type of level shift circuit (e.g. one having four transistors) with another functionally equivalent type of level shift circuit (e.g. one having six transistors) is well known to those of ordinary skill in the art.

Therefore, no claim is allowable as presently written.

Allowable Subject Matter

However, claim 4 is only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure the switch circuit comprises the switching element and capacitor as cited within claim 4.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln D. Donovan, can be reached on (571) 272-1988

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/T.L.E./

Examiner, Art Unit 2816

/Donovan Lincoln/

Supervisory Patent Examiner, Art Unit 2816